ULTRA THIN BODY

VERTICAL REPLACEMENT GATE

MOSFET

ABSTRACT OF THE DISCLOSURE

A method of fabricating a VRG MOSFET includes the steps of: (a) forming a VRG multilayer stack; (b) forming a trench in the stack; (c) depositing an ultra thin, amorphous semiconductor (α-semic) layer on the sidewalls of the trench (portions of the ultra thin layer on the sidewalls of the trench will ultimately form the channel or ultra thin body (UTB) of the MOSFET); (d) forming a thicker, α-semic sacrificial layer on the ultra thin layer; (e) annealing the α-semic layers to recrystallize them into single crystal layers; (f) selectively removing the recrystallized sacrificial layer; and (g) performing additional steps to complete the VRG MOSFET. In general, the sacrificial layer should facilitate the recrystallization of the ultra thin layer into single crystal material. In addition, the etch rate of the sacrificial layer should be sufficiently higher than that the ultra thin layer so that the sacrificial layer can be selectively removed in the presence of the ultra thin layer after recrystallization. The latter condition is illustratively satisfied by doping the sacrificial layer and by not (intentionally) doping the ultra thin layer. In accordance with one embodiment of our invention, step (g) includes filling the trench with oxide to form a thick *back oxide* region. In accordance with another embodiment of our invention, step (g) includes depositing a thin oxide layer (the *back oxide*) in the trench and then filling the remainder of the trench with a polycrystalline region (the *back gate*). VRG MOSFETs fabricated in accordance with our invention are expected to be electrostatically scalable with precise dimensional control. In addition, they can be fully depleted. Novel UTB device designs are also described.